Influence of solvent additive on the performance and aging behavior of non-fullerene organic solar cells

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ABSTRACT

The performance of organic solar cells has improved significantly in recent years due to the use of non-fullerene acceptors (NFA). While processing additives are typically added to the active layer blends to enhance device performance in NFA organic solar cells, their impact on device degradation remains unclear. In this work we have compared the performance, in pristine and degraded state, between air-processed slot-die coated NFA ITO-free organic solar cells with and without the processing additive DIO, using a structure of PET/Ag/ZnO/PBDB-T:ITIC/FHC PEDOT:PSS. We observed an improvement in the power conversion efficiency of the devices when adding DIO, from 4.03% up to 4.97%. The evolution of the performance for both devices under ISOS-L1 life testing protocol reveals that the drop in efficiency is mainly due to a decay of J_{SC} for both cells. In the short time scale the efficiency of non-DIO cells decays faster than the DIO cells, whereas in the long time scale the efficiency of non-DIO cells tends to stabilize sooner. Carrier mobilities estimated from impedance measurements decrease with time at similar rate for both degraded samples. Besides, DIO devices present a steep increase of the series resistance with time causing a decrease of the FF and thus of the efficiency. Moreover, in both degraded devices, the open-circuit voltage saturates with increasing illumination intensity. Numerical simulations reveal that a reduced anode work function of 5 eV is needed to fit experimental data.

1. Introduction

Organic solar cells (OSCs) have achieved a certified power conversion efficiency (PCE) of 18.6% (Cai et al., 2021) and they appear to be promising alternatives in thin film photovoltaic technology (Kang et al., 2016). Potential advantages are low-cost and ease of processing, non-toxic materials, full design flexibility and semi-transparency, and its integration onto flexible substrates given the existence of a vast variety of organic structures with tunable functionalities. A critical issue in OSCs is properly mixing the electron donor (D) and the electron acceptor (A) to form an active layer blend resembling a network of D/A materials with nanoscale heterojunction interfaces, the so-called bulk heterojunction (BHJ). These systems ensure that all photogenerated excitons reach a D/A interface within their diffusion length. Fullerene derivatives such as $PC_{60}BM/PC_{70}BM$ have been extensively used in BHJ as electron acceptors. However, they exhibited limited PCE, rarely above 10% (Ganesamoorthy et al., 2017), as a result of limited light absorption and limited open-circuit voltage (V_{OC}) due to difficulties in electronic levels tunability. In the past years, non-fullerene acceptors (NFA) have emerged as ideal candidates due to their easy synthesis, strong absorption coefficient extending up to near-infrared, tunable electronic properties, and enhanced stability. Previous works reported single junction NFA solar cells with PCE up to 18% in single junction solar cells (Wang et al., 2019; Cui et al., 2019; Li et al., 2018; Fan et al., 2019; Zhang et al., 2018).

Moreover, bulk morphology plays an important role in charge transport in BHJ solar cells, and it can be controlled by modifying factors such as the solvent, drying conditions, device annealing, or a more recent strategy, including small concentrations of additives in the solvents (Araújo et al., 2019; Song et al., 2018; Yang et al., 2020). The latter

strategy has been widely explored in BHJ, in particular, the effect of adding 1,8-diiooctane (DIO) to the solvent since it allows morphological control of the active layer. The addition of DIO in systems with a fullerene acceptor reduces the domain size of the $PC_{60}BM/PC_{70}BM$, increasing crystallinity and reducing the internal resistance. As a result, the D/A interface is optimized, achieving highly efficient exciton dissociation, improved charge carrier mobility, and ultimately enhanced PCE (Araújo et al., 2019; Song et al., 2018; Yao et al., 2014; Liao et al., 2013).

Previous works have also studied the effect of adding DIO to NFA blends; however, the benefits still remain unclear for this type of systems. Several studies have compared the effect of adding a 3% concentration of DIO to fullerene blends versus NFA systems based on the electron acceptor ITIC, using polymers PBDB-T and PTB7-Th as donors. They observed a positive effect in the PTB7-Th:$PC_{71}BM$ blends, but a dramatic drop in performance for NFA devices (Song et al., 2018; Doumon et al., 2019). However, Xie et al. found that the PCE for NFA PBDB-T:m-ITIC solar cells is maximized when the DIO concentration is optimized. They obtained a PCE of 11.1% for DIO concentration 0.5%, compared to PCE of 10% for DIO concentration 3%. They attributed the improvement mainly to favorable film morphology that enables optimized fill-factor (FF) (Xie et al., 2019). Therefore, the effect of adding DIO in NFA systems on the performance as well as on the stability of such systems is still under debate, and further investigation needs to be carried out.

In this work we have compared the performance and stability in fully scalable NFA devices with active layer PBDB-T:ITIC, with 0.5% DIO in the solvent versus the same blend without DIO. The device structure is PET/Ag/ZnO/PBDB-T:ITIC/FHC PEDOT:PSS, and devices are fabricated on flexible substrates by slot-die coating in air. Samples were characterized in AC by impedance spectroscopy (IS) and simulated with a lumped parameter model. Indoor lifetime testing was carried out according to the International Summit on Organic Photovoltaic Stability (ISOS) standard L-1 protocol (Reese et al., 2011). Finally, we have performed 2D numerical device simulations using SILVACO ATLAS TCAD to support our conclusions about the enhancement of carrier mobility in DIO devices, and to help understanding the different ideality factors measured in both types of cells.

2. Experimental methods

2.1. Device fabrication

Device layout and layer structure is presented in Fig. 1a. Heat stabilized PET was used as a substrate (125 μm, Melinex ST504, DuPont Teijin Films). ZnO nanoparticles were used as electron transport layer (Genes'ink H-SZ01034) and ink was in-line filtered with a 0.2 μm PS filter from Whatman. The active layer solution was prepared with a ratio 1:1 (PBDB-T: ITIC, Brilliant Matters Inc.) at a total concentration of 20 mg/ml in chlorobenzene with 0.5% v/v of 1,8-diiodooctane. The solution was stirred at 90 °C for 3 h in ambient conditions. PEDOT:PSS (FHC Solar, Heraeus) was diluted with isopropanol (1:1 ratio) prior to coating

and stirred at room temperature for approximately 30 min.

OSCs were fabricated with inverted device configuration as seen in Fig. 1b (PET/Ag/ZnO/PBDB-T:ITIC/FHC PEDOT:PSS). Prior to silver deposition, the PET substrates were pretreated with DC argon plasma in vacuum. Silver electrodes (~100 nm thickness) were deposited using DC magnetron sputter (power 150 W, pressure ~ 6×10^{-3} mbar, time 170 s), through a shadow mask that defines the cell layout. PET foil dimensions were 350 mm × 100 mm containing electrodes for 60 samples sputter deposited in four rows. Each sample contained four devices that had an active area of 5.4 mm^2. Further solution processing for device fabrication was performed in ambient atmosphere and slot-die sheet coater was used. For the coating process, a motorized thin film applicator (Erichsen COATMASTER 510) was modified to use custom-made stainless-steel slot-die head. The coating system holds a vacuum plate containing a heating element and a syringe pump for controlled ink delivery. In addition, during coating process syringe can be heated in an aluminum sleeve with silicone heater pads and slot-die head can be used in elevated temperatures by using heating cartridge. For the electron transport layer (ETL) and active layer, shim and meniscus guide were used to limit the coating width to 11 mm. For the FHC PEDOT:PSS coating width was limited to 7 mm. Details regarding the fabrication process and layer thicknesses can be seen in Table 1.

For all the slot-die coated layers substrate temperature was kept at 75 °C. Furthermore, during the active layer coating, slot-die head and the syringe holder were heated to 65 °C. Annealing for the devices was performed in vacuum oven. As a last process step, samples were cut from the foil and glued (Permabond 105) on glass substrate followed by encapsulation with a round glass cover. Delo KATIOBOND LP655 was used as encapsulation glue (UV-curable).

2.2. Characterization methods

Current density–voltage *(J-V)* curves were performed with a Keithley 2450 from −0.3 to 1.2 V for different light intensities from 5 up to 100 mW/cm^2 using a Newport Oriel VeraSol-2 light-emitting diode (LED) class AAA solar simulator calibrated with an NIST-certified KG5 filtered Si reference cell. *J-V* curves in dark conditions were also measured. The PCE of the fabricated devices under AM1.5G spectrum was determined.

Electrical measurements were carried out using an Auto-Lab potentiostat/galvanostat model PGSTAT204 (Metrohm), equipped with the

Table 1
Fabrication process parameters.

Layer	Pumping speed (ml/min)	Coating speed (mm/s)	Coating gap (μm)	Thickness (nm)	Annealing
ZnO	0.05	12	200	~30	100 °C (10 min)
PBDB-T:ITIC	0.035	6.3	200	~200	–
FHC Solar	0.16	12	100	~220	100 °C (5 min)
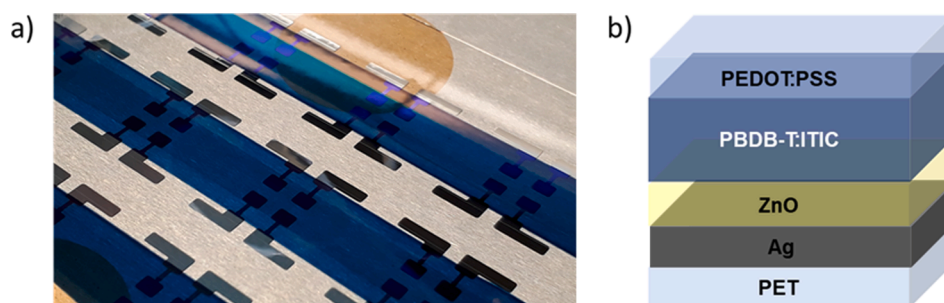
Fig. 1. a) Device layout and b) layer structure.

FRA32M impedance module and the Metrohm AutoLab optical bench. The instrument was driven by the NOVA 2.1.4 software. IS measurements were carried out configuring AutoLab to apply sinusoidal signals with a 50 mV amplitude from 1 MHz to 1 Hz under open-circuit conditions. The fits of all the impedance spectra were performed using Scribner's ZView software.

External quantum efficiency (EQE) was estimated using VeraSol-2 LED solar simulator for both pristine and degraded devices, measuring the spectral response at every LED wavelength. The measurements were made from 420 up to 1050 nm, measuring 19 different wavelengths.

Indoor lifetime testing was carried out according to the ISOS standard L-1 protocol. During these experiments, devices were exposed to 1 sun AM1.5G illumination under controlled temperature and humidity conditions. VeraSol-2 LED solar simulator was used as illumination source. *J-V* measurements were monitored every 5 min for a period of 70 h for fast life testing, and impedance spectra were measured once a day for 450 h. Devices were characterized by IS under dark conditions and under illumination during the degradation process. Finally, the characterization was performed on four samples (two DIO samples and two non-DIO samples), with four devices each, that is, 8 nominally equal devices of each type.

As we mentioned before, the cells presented in this work are developed under industrial conditions from scalable processes in air (S2S slot-die coating), using flexible substrates (PET foil) and ITO-free electrodes. Therefore, the expected efficiency is lower than the typically reported for this active layer material system using ITO as electrode or glass substrates. However, the aim of this work is not to achieve high efficiency, but to investigate the stability and compare the degradation pathways of cells fabricated with and without DIO.

3. Results and discussion

Fig. 2 shows the *J-V* characteristics under AM1.5G illumination for two fresh samples (with and without DIO) and Table 2 summarises the DC cell parameters obtained from these *J-V* curves. DIO devices show an increased short-circuit current (J_{SC}) of approximately 5% compared to the non-DIO devices. As mentioned earlier, when DIO is added to the solvent the structure crystallinity increases, which ultimately improves carrier mobility. The V_{OC} increases around 30 mV for DIO devices. This is probably due to the change in mobilities and electrode work functions, which will be supported by 2D numerical simulations at the end of this section. The non-DIO devices also present a reduced value for the FF of 0.47 compared the 0.53 for the DIO devices. These low FF values can be explained by the *J-V* being dominated by a series resistance mechanism,
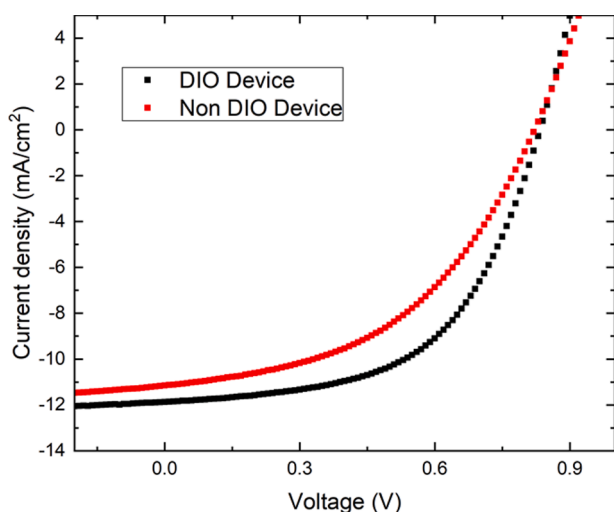

Fig. 2. *J-V* curves of pristine devices with and without DIO under simulated AM1.5G (100 mW/cm^2) irradiance.

Table 2
Photovoltaic average parameters of pristine DIO and non-DIO devices under AM1.5G illumination.

	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	PCE (%)
DIO cell	0.811 ± 0.006	11.56 ± 1.41	52.7 ± 2.4	4.97 ± 0.83
Non-DIO cell	0.783 ± 0.015	11.02 ± 0.64	46.6 ± 2.0	4.03 ± 0.47

as expected due to the ambient slot-die fabrication process on flexible substrates with relatively thick active layers. These cell parameters result in an average PCE of 4.97% and 4.03% for DIO and non-DIO devices, respectively, and the PCE obtained for the champion cells were 6.19% and 4.69% for DIO and non-DIO devices, respectively.

These differences in the *J-V* curves of samples with and without DIO suggest that indeed DIO alters the morphology of the active layers leading to different physical mechanisms, or dynamics hereof, taking place inside the devices.

Table 3 shows the ideality factors (*n*) for both types of devices in pristine conditions obtained from the slope of the logarithmic fit of the V_{OC} vs illumination intensity (irradiance) curve. Surprisingly, low ideality factors of 1.07 and 0.70 are obtained for DIO cells and non-DIO cells, respectively. A low ideality factor does not necessarily indicate a good device performance. According to Tress et al., in the case of non-selective contacts V_{OC} saturates with light intensity, and therefore ideality factor is lower than one, indicating surface recombination (Tress et al., 2018). In the case of DIO cells, the value of 1.07 may indicate Shockley Read Hall (SRH) recombination in the bulk near the anode contact, where the light is strongly absorbed.

To gain insight into the recombination mechanisms, we performed an indoor lifetime testing according to ISOS standard L-1 protocol. Devices were continuously exposed to 1 sun AM1.5G illumination under room temperature, and the *J-V* in dark and under illumination were recorded periodically. Fig. 3 shows the evolution of the normalized cell parameters for both type of devices. The drop in the PCE is mainly due to the decrease in J_{SC} that decays approximately 30% and 35% during 60 h for the DIO and non-DIO devices respectively, while interestingly the V_{OC} remains almost unchanged for both types of devices. On the other hand, it is worth mentioning that FF slightly increases for non-DIO devices, maybe due to a slightly altered morphology with illumination, while it decays for DIO cells indicating that additional effects play a role here. This can be explained since the latter devices present a higher current, and therefore, are strongly dominated by a series resistance phenomenon that worsens during the degradation process. The increase of series resistance for DIO cells will be later confirmed by IS. Introducing DIO in small amounts slows down the efficiency decay at initial stages, however, after the first 20 h of operation, the efficiency for non-DIO devices remains constant, while it continues to slightly decrease for DIO devices, which is attributed to the same trend of the FF and, in a less extent, to J_{SC}. *J-V* monitoring was stopped every day for around 30 min to measure the impedance spectra, which explains the noisy points every 24 h in Fig. 3.

The relative EQE for both type of devices in pristine conditions exhibits a first maximum at approximately 530 nm and a second one at around 690 nm, as shown in Fig. 4. As expected, the EQE decreases for degraded samples, and the drop for both types of devices is higher in the red zone of the spectrum. In particular, at 630 nm it drops 45% and 35% for non-DIO and DIO devices, respectively, while at 420 nm it drops around 33% and 25% for non-DIO and DIO devices, respectively. Previous studies for similar active layers reported that the absorption in the

Table 3
Ideality factors obtained from the logarithmic fit of V_{OC} vs light intensity for both types of devices.

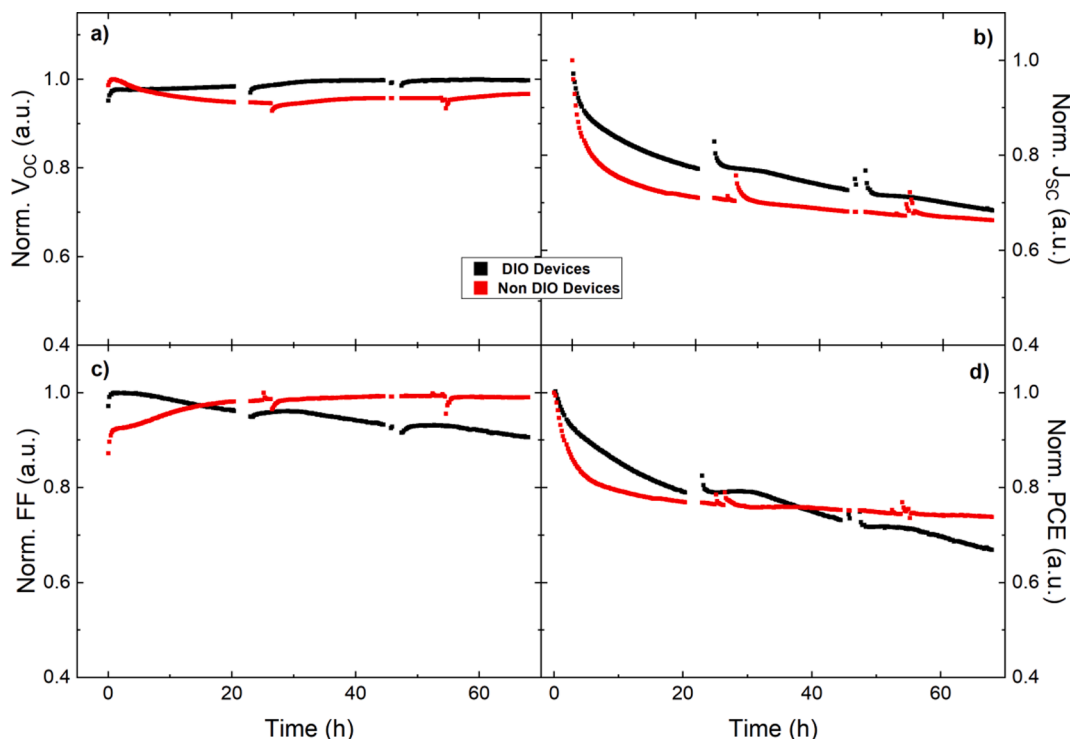|	DIO	Non-DIO
Ideality factor	1.07 ± 0.04	0.70 ± 0.05

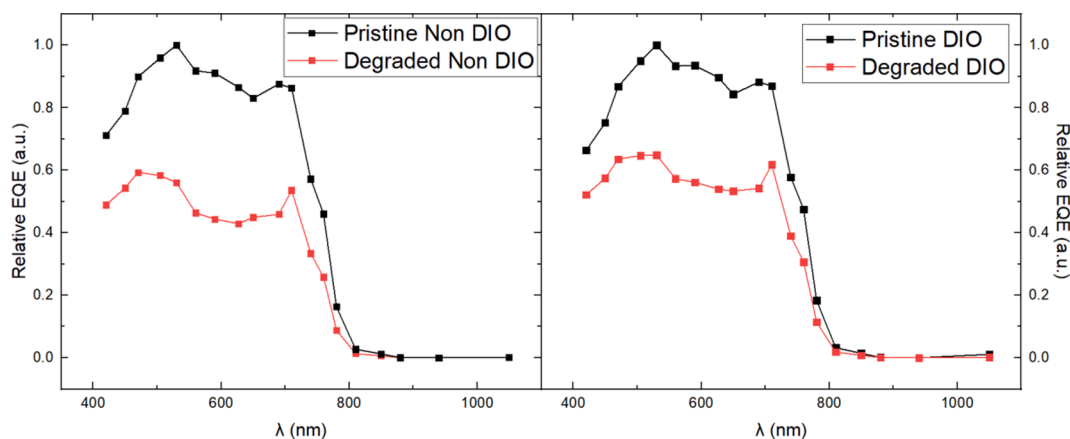**Fig. 3.** Evolution of the normalized cell parameters with time during ISOS-L1 life testing protocol.

Fig. 4. Relative external quantum efficiency (EQE) normalized to the maximum value for pristine and degraded samples for DIO and non-DIO devices.

red part of the spectrum is much more intense than in the blue region (Zhao et al., 2016; Destouesse et al., 2019), and from the Beer-Lambert law it is deduced that the red light is absorbed more intensely near the anode contact, while blue light penetrates deeper in the layer. The fact that the EQE diminishes more strongly in the red region for both samples indicates that devices are degrading more severely near the anode, as already reported for similar samples in a previous work (Arredondo et al., 2020).

Impedance spectra in dark conditions from 1 MHz to 1 Hz were measured for both type of devices in pristine and degraded conditions. Experimental data exhibit the typical semicircle that can be accurately fitted with a simple parallel RC circuit. The overall capacitance has been extracted from the Cole-Cole curves in dark conditions at reverse and low forward bias. The capacitance extracted from the fit follows a voltage dependence according to Mott-Schottky expression $C^{-2} = \frac{2(V_{bi}-V)}{A^2 \varepsilon \varepsilon_0 N_A}$, and therefore it is attributed to the depletion capacitance due to band bending at the cathode contact.

Fig. 5 shows the linear fit C^{-2} vs V resembling a typical Mott-Schottky behaviour. From this fit, the acceptor impurity density (N_A) displayed in Table 4 for both type of samples in pristine and degraded conditions is obtained. It is observed that N_A is slightly higher for non-DIO devices than for DIO devices. Analysis with degradation time reveals that N_A slightly increases for both types of devices, that is, barely 4% for DIO devices and 10% for non-DIO devices. This indicates that no significant acceptor impurity density (that eventually may act as trapping centres) is introduced near the cathode contact along degradation, particularly in DIO devices. That is, the cathode interface ZnO/active layer, shielded by the PET/Ag back contact, does not appear to be severely affected after 312 h of operation.

The dielectric constant (ε) of the active layer blend is estimated from the geometrical capacitance C_g at -0.3 V as $\varepsilon = C_g L / A \varepsilon_0$, with active layer thickness L = 200 nm and device area A = 5.4 mm^2 and ε_0 the vacuum permittivity, leading to values of 5.5 and 4.6 for DIO and non-DIO samples, respectively. The higher values of ε for DIO samples,
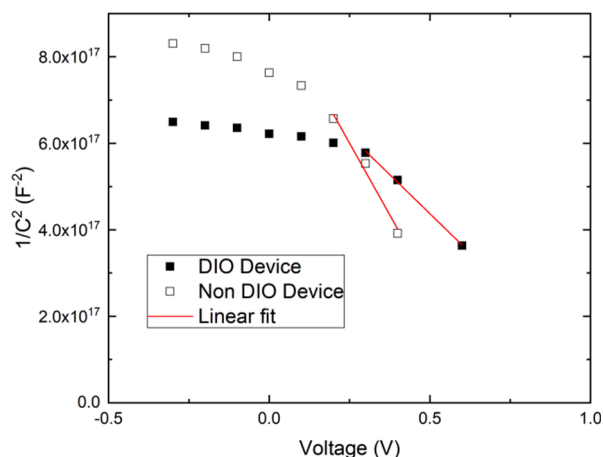
Fig. 5. Mott–Schottky plots for the two types of cells for pristine state.

Table 4
Acceptor density obtained from the Mott-Schottky analysis at different degradation stages.

N_A (x10^{22} m^{-3})			
Time (h)	**0**	**72**	**312**
DIO cells	1.8	1.87	1.88
Non DIO cells	2.97	3.12	3.26

around 20%, indicate a better quality of the blend, in terms of crystallinity and morphology.

Fig. 6 shows the impedance spectra for DIO (a) and non-DIO cells (b) at V_{OC} (under 1 sun of illumination) for pristine and degraded samples (at two different stages of the degradation process, after 6 and 14 days under constant 1 sun irradiation). Symbols correspond to the experimental data and lines are the best fits using the Matryoshka circuit (see inset of Fig. 6). The circuit is composed of an R_P-CPE (constant phase element) network, that models the charge recombination at the bulk, in series with a high frequency resistance, R_T, related to charge transport, and a parallel capacitance, C_g, which represents the geometrical capacitance of the blend, related to the active layer dielectric constant. The CPE is used in order to fit a depressed semicircle, and models a non-

ideal capacitance behaviour, whose impedance is given by $Z_{CPE} = 1/[(j\omega)^{\alpha}Q]$. As explained in (Arredondo et al., 2020), the parameter Q (non-ideal chemical capacitance) is related to the effective chemical capacitance of the CPE element, C_{μ}, given by $R_P^{(1-\alpha)/\alpha}Q^{1/\alpha}$. When the exponent α approximates to 1, the CPE approximates an ideal capacitor.

Both figures show a similar trend, i.e., semicircles increase with the degradation time. This tendency implies an increase of the device dynamical resistance, due to a decrease of the photogenerated current as OSC degrades.

Fig. 7 shows the time evolution of the circuital parameters (R_T, R_P, Q and C_g) for DIO (black symbols) and non-DIO (red symbols) devices at V_{OC} under 1 sun. Transport resistance, shown in Fig. 7a, is around 20% higher for non-DIO samples, indicating a lower mobility in these devices, compared to DIO-samples. This resistance displays a slight increase with degradation time, which indicates a worsening of the blend conductivity. Fig. 7b shows an increase of the recombination resistance (R_P) with degradation time for both samples. This behavior is due to the decrease of the J_{SC} as the cell degrades, since the dynamical resistance at V_{OC}, dominated by R_P, is inversely proportional to the photo-generated current. In order to investigate the effect of DIO in carrier recombination, R_P has been plotted versus J_{SC} in the inset, so that recombination can be evaluated at the same photocurrent level. We can observe that R_P is higher for the DIO cells, indicating a lower carrier recombination for these devices. The non-ideal chemical capacitance Q is slightly smaller for DIO cells reinforcing the idea of an improved blend crystallinity. Moreover, Q does not significantly change with time for both samples, indicating that the incorporation of DIO does not affect blend degradation. Geometrical capacitance (see Fig. 7d) is higher for DIO samples as corresponds for a greater blend dielectric constant, and it remains constant with time for both types of cells. The values of C_g shown in Fig. 7d for pristine devices are slightly higher than those obtained from Mott-Schottky analysis (obtained from C at reverse bias under dark conditions) which is typically attributed to device heating when measuring under illumination conditions.

It is worth noting that the series resistance obtained from the fit increases more steeply for DIO cells. Both devices show series resistance around 100–120 Ω in the pristine state, and after 125 h under continuous illumination, the non-DIO cells show 150 Ω whereas DIO cells show R_S above 450 Ω as shown in the inset of Fig. 7a. In the case of DIO devices, that show a higher photocurrent, the device is strongly dominated by a series resistance, which is directly related to the decrease of the FF. It is worth noticing that Rs is shown only up to 150 h. For very degraded
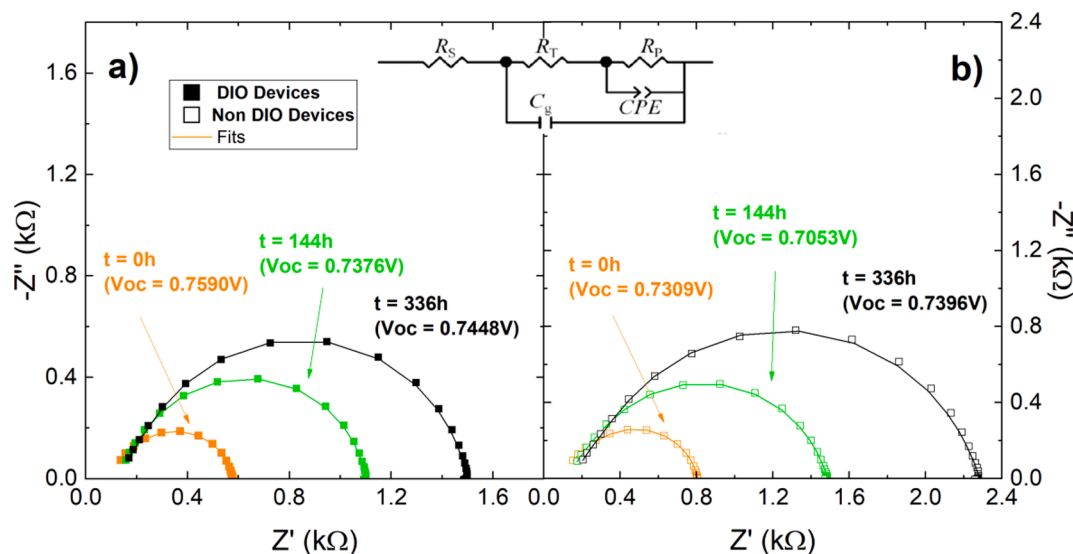

Fig. 6. Impedance spectra under 1 sun illumination for non-DIO (open symbols) and DIO (fill symbols) devices at different degradation stages. Solid lines show the fits using the circuit of the inset.
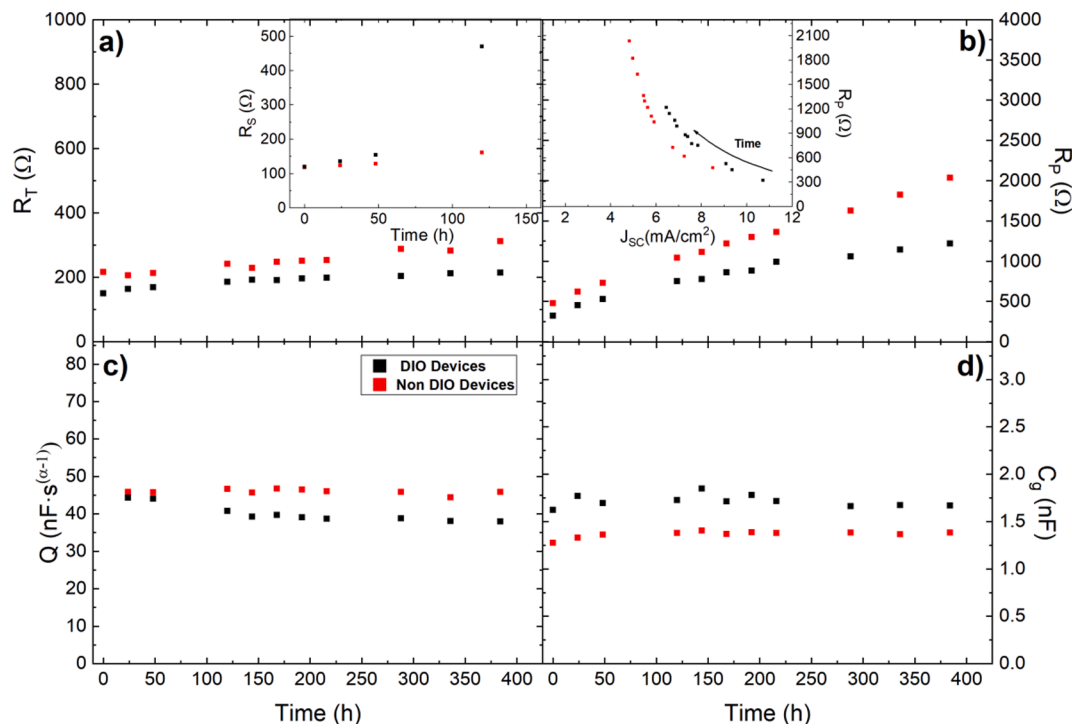
Fig. 7. Evolution with time of circuital parameters obtained from the fit of Fig. 6 for both type of devices. Inset of figure b) shows the evolution R_P versus J_{SC}.

samples, the relative error of this parameter is non-negligible since at high frequency (where the Rs is extracted) and at high degradation stages (t > 150 h), the measurements are noisier and an additional inductive behavior usually occurs. Whereas the evolution of the Rs in the inset may serve as a guideline, the absolute value of Rs obtained from the fit, especially at high degradation times, may present great uncertainty.

Finally, diffusion time has been obtained using the expression $\tau_D = R_T C_\mu$ and minority carrier mobility can be evaluated for both types of cells at different degradation stages as $\mu = \frac{eL^2}{\tau_D kT}$ (see Fig. 8). In both samples, mobility decreases with degradation, as expected. Moreover, mobility is around 50% higher for DIO samples, indicating that carrier transport is improved when adding DIO, as anticipated for a blend with enhanced crystallinity. It is worth noting that whereas the trend of the mobility shown in Fig. 8 may serve as indication of blend crystallinity, the absolute value of μ obtained from the impedance may present great

uncertainty. Moreover, Fig. 8 shows that the decreasing slope of the active layer mobility is similar in both samples, indicating that both blends degrade at similar rates. However, the fact that the series resistance increases more steeply for the DIO cells, suggests that the conductivity is worsening faster in this type of cells. Wang et al. reported that DIO leads to chemical degradation at the PEDOT:PSS interface, chemically reducing this layer and lowering its work function (Wang et al., 2020). Thus, since according to the mobility evolution with time both blends degrade at the same rate, the increase of the series resistance for DIO cells may indicate that the chemical reduction of PEDOT:PSS may also decrease the conductivity of this layer, worsening lateral conduction. This could explain the higher drop of FF for the DIO cells at long time scales, and ultimately, the non-stabilization of the PCE.

Finally, we performed 2D numerical simulations using the commercial software Silvaco ATLAS TCAD to compare the effect of degradation between both types of devices. Details about the device structure and material parameters used for the simulations can be found in (Arredondo et al., 2020).

Fig. 9a shows the comparison between experimental and simulated *J-V* under 1-sun illumination and EQE (inset) for degraded DIO and non-DIO devices. Simulations are in good agreement with experiment for both types of degraded devices when the minority carrier mobilities are reduced to 20% of the pristine values (around 3.5×10^{-2} and 2.5×10^{-2} cm^2/(Vs), for DIO and non-DIO respectively, see Fig. 8). Besides, the hole transport layer, HTL (PEDOT:PSS) work functions obtained from the fits are 5.03 eV and 5 eV for DIO and non-DIO degraded cells, respectively. Indeed, EQE (and, thus, J_{SC}) can be accurately fitted with values obtained from Table 5, indicating that, although both mobilities decrease for degraded samples, they do it in the same proportion, and thus, in degraded conditions the mobility is still 60% higher for DIO cells, in consonance with the hypothesis of improved morphology in the DIO devices. In addition, we can observe that V_{OC} barely changes with illumination intensity for both type of degraded samples. Simulations reproduce this behavior when the HTL (PEDOT:PSS) work function WF_A (i.e. Fermi level position with respect to vacuum level) is around 5 eV or lower. For higher WF_A, in particular for work functions that match or surpass the quasi-Fermi level of holes of the active layer, the V_{OC}
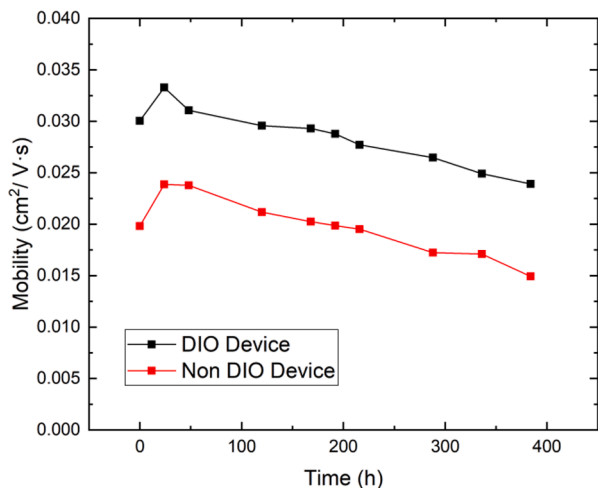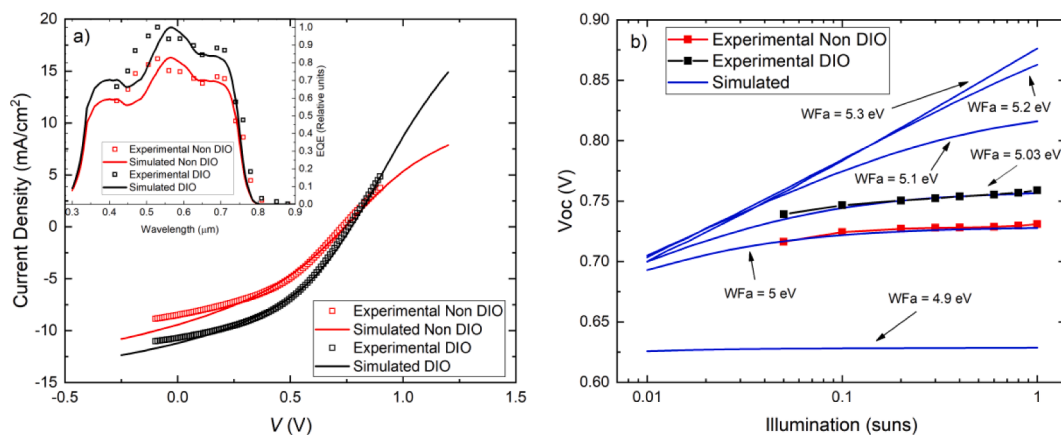

Fig. 8. Temporal evolution of minority carrier mobility for both types of cells obtained from impedance measurements.

Fig. 9. a) Experimental *J-V* under 1-sun illumination (symbols) and simulations (solid lines) for degraded devices. Inset shows the experimental and simulated EQE for DIO and non-DIO devices. b) Simulated V_{OC} vs illumination intensity for different anode work functions (solid lines) and experimental data for DIO and non-DIO degraded devices (symbols).

Table 5

Carrier mobilities and HTL work functions extracted from the fits of degraded samples using Silvaco ATLAS TCAD.

	DIO Devices	Non-DIO Devices
Minority carrier mobilities ($cm^2V^{-1}s^{-1}$)	8×10^{-3}	5×10^{-3}
HTL (PEDOT:PSS) work function (eV)	5.03	5.00

strongly increases with light intensity, as expected and as shown in Fig. 9b, and in general reach higher values. In fact, for values of $WF_A = 5$ eV or lower (degraded devices), simulations show a change in the direction of the internal electric field near the anode, which in turn causes a hole depletion region since hole transport is no longer drift assisted towards the electrodes. This change in the sign of the electric field ultimately results in the quasi-Fermi level of holes to pin at the HTL interface under illumination at V_{OC}. This quasi Fermi-level pinning for degraded devices is the reason for the saturation of V_{OC} as the light intensity increases. Moreover, this constant V_{OC} vs light has a great impact in the ideality factor, while in pristine devices we obtain values of 1.07 and 0.70 for DIO and non-DIO cells (see Table 3), for degraded samples *n* drops below 0.4 in both types of devices.

4. Conclusions

We have compared the performance between devices with the structure PET/Ag/ZnO/PBDB-T:ITIC/FHC PEDOT:PSS adding 0.5% DIO to the solvent blend, and DIO free cells with the same structure. In the pristine state, DIO cells show a better performance with efficiency 4.97% compared to 4.03% of non-DIO samples. The mobilities obtained from impedance measurements are 3.5×10^{-2} cm^2/(Vs) and $2.5 \times 10^{-2} cm^2$/(Vs), for DIO and non-DIO blends respectively, indicating an increased crystallinity when DIO is added, which ultimately improves carrier conduction in pristine state.

Moreover, we have compared the evolution of performance for both devices under ISOS-L1 life testing protocol. In the first hours of operation, DIO cells show a less pronounced burn-in than non DIO devices, however, the efficiency of DIO devices keeps lowering at longer timescales in contrast to non DIO samples, where it remains constant after 20 h of operation. The non-stabilization of the efficiency for DIO cells is due to the FF that follows the same trend. Circuital modeling of impedance measurements reveals a stronger increase of the series resistance for the DIO cells during the degradation process, which, together with the higher photocurrent, indicates that these devices are strongly dominated by series resistance, causing the decrease of the FF. Moreover, mobility decreases at the same rate for both type of degraded

samples, suggesting that the incorporation of DIO improves the initial morphology, and it does not affect the degradation evolution of the blend. Therefore, the increase in series resistance for the DIO cells indicates that the PEDOT:PSS layer shows a drop in conductivity upon degradation, as a result of chemical interaction with DIO. This conductivity decrease can worsen lateral conduction, which in turn causes the decrease of the FF and ultimately of the device power conversion efficiency.

Besides, we observe that for both degraded cells, V_{OC} barely changes with illumination intensity. The *J-V* curve and EQE of degraded samples have been successfully reproduced using Silvaco ATLAS TCAD, and we have obtained an anode WF_A of around 5 eV to fit the experimental data. Simulations reveal that for this value of WF_A (or lower) the quasi-Fermi level of holes pins at the anode/active layer interface, causing a change on the direction of the internal electric field near the anode, and the saturation of V_{OC} as the light intensity increases.

We conclude that the incorporation of process additives improves the initial morphology of the active layer and thus device performance. However, they have a negative impact on the long-term device stability in this type of configuration. On one hand, the additive triggers a chemical reaction with PEDOT:PSS increasing series resistance, and lowering conductivity and FF. On the other hand, the V_{OC} saturates with increasing light intensity due to the pin of the hole quasi-Fermi level at the HTL interface. Therefore, the use of such process additives in upscaled OPV should be carefully considered. It may benefit on the short term but has a negative impact on the longer term. Further research needs to be carried out before its application to real life installations.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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